REMARKS

Claims 1-8 were pending in the above referenced application. Claims 1 and 5 are amended and Claim 50 has been added. Therefore claims 1-8 and 50 remain in the application for consideration.

In addition, Applicant requests that the Examiner indicate in the next action whether or not the drawings for this application, submitted February 24, 2000, have been approved.

Objected to Claims

Claim 5 stands objected to because of the following informalities: in claim 5, line 3, a phrase "conductive material" should be changed to "a conductive material". Applicant has amended the claim in accordance with the Examiner's suggestion and notes that such amendment does NOT change the scope of Claim 5. The amendment being made, the objection is now moot.

Rejection under 35 U.S.C. §103

Mano in view of Wolf

Claims 1-8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Mano (US 5,814,886) in view of Wolf (Vol. 3) (hereinafter "Wolf"). Applicant traverses.

Claims 1 and 5 both recite "the conductive line not being a gate electrode." In contrast, Mano at col. 2, lines 63-65 specifically discloses that "[t]he interconnections L1 and L2 are connected to the gate electrodes G1 and G2 by shared contacts C1 and C2." Thus the conductive line **not** being a gate electrode is neither disclosed or even suggested by Mano. With regard to Wolf, the teaching highlighted by the Examiner as germane is also directed to contacts encompassing a gate electrode, specifically the gate electrode of a MOSFET. Hence like Mano, the conductive line **not** being a gate electrode is neither disclosed or suggested.

It is shown above that both Mano and Wolf teach interconnection to a gate electrode. Claims 1 and 5 specifically exclude a gate electrode. Referring to

MPEP: 2143.03, one is instructed that to maintain a rejection under §103, "All Claim Limitations Must Be Taught or Suggested" by the cited art. Since neither Mano or Wolf individually disclose or even suggest the element of the instant invention "the conductive line not being a gate electrode," there CANNOT be a combination of such art that can be fairly said to provide such a disclosure or suggestion. Therefore, the rejection of Claims 1 and 5 are in error and MUST be withdrawn. For at least the same reason, the rejection of Claims 2-4, 50, and 6-8 depending from Claims 1 and 5, respectively, is also in error and MUST be withdrawn. Action to this effect is requested.

En in view of Wolf

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Claims 1-8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over En et al (US 5,990,524) (hereinafter "En") in view of Wolf. Applicant traverses.

As stated above, Claims 1 and 5 both recite "the conductive line not being a gate electrode." The Examiner alleges that the En and Wolf make the invention of Claims 1 and 5 obvious. Turning first to En, the structure shown in the referred to Fig. 4, depicts a conductive plug 50 in electrical contact with **gate electrode 16** through conductive glue layer 48 and conductive silicide 18, (see, col. 7, lines 1-47). Thus, similar to the disclosure of Mano, En also only discloses or suggests contact to a gate electrode.

Referring to Wolf, the Examiner makes the same allegation in the instant rejection as for the rejection incorporating Mano, thus Applicant reasserts the argument above herein.

Thus, it is shown that both En and Wolf teach interconnection to a gate electrode. Claims 1 and 5 specifically exclude a gate electrode. Again referring to MPEP: 2143.03, since neither En or Wolf individually disclose or even suggest the element of the instant invention "the conductive line not being a gate electrode," there CANNOT be a combination of such art that can be fairly said to provide such a disclosure or suggestion. Therefore, the rejection of Claims 1 and 5 are in error and MUST be withdrawn. For at least the same reason, the rejection of Claims 2-4, 50, and 6-8 depending from Claims 1 and 5,

respectively, is also in error and MUST be withdrawn. Action to this effect is requested.

In summary, Applicant having responded to each of the rejections and objections, respectfully asserts that Claims 1-8 and 50 are in condition for allowance. Action to that effect is earnestly sought. If, however the Examiner's next action is anything other than a Notice of Allowance, the Examiner is requested to call the undersigned to schedule a telephonic interview. The undersigned is available during normal business hours, Pacific Coast Time.

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Respectfully submitted,

Dated: See 2, w

Bernard Berman

EL84405 043

IN THE UNITED STATES PATENTY

Application Serial No.	
Filing Date	
Inventor	Robert Kerr et al.
Assignee	Micron Technology, Inc.
Group Art Unit	2814
Examiner	P. Cao
Attorney's Docket No	MI22-1343
Title: Methods of Forming Contacts, Methods of Contacting Lines, Methods of	
Operating Integrated Circuitry, and Integrated Circuits	

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING **RESPONSE TO September 4, 2001 OFFICE ACTION**

The claims have been amended as follows. <u>Underlines indicate insertions</u> and strikeouts indicate deletions.

- An integrated circuit comprising a conductive line, the conductive line not being a gate electrode, received over a semiconductive substrate and a diffusion region within the substrate proximate the line, the diffusion region and substrate forming a junction which is effectively reverse biased to preclude shorting between the conductive line and the substrate through any conductive material extending therebetween for selected magnitudes of current provided through the conductive line.
- 5. An integrated circuit comprising a conductive line received, the conductive line not being a gate electrode, over a semiconductive substrate and a diffusion region within the substrate proximate the line, a conductive material being received over the line and interconnecting it with the diffusion region, the diffusion region being effectively reverse biased to preclude shorting between the conductive line and the substrate through the conductive material for selected magnitudes of current provided through the conductive line.

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